CLAIMS

1. A cell array comprising a plurality of cells, each cell including a selection bipolar transistor and a storage component, each said bipolar transistor having a first, a second and a control region, and each said storage component having a first and a second terminal, said first region of each bipolar transistor being connected to said first terminal of a respective storage component, said cell array comprising a body of semiconductor material including:

a common region of a first conductivity type, forming said second regions;

a plurality of active area regions of a second conductivity type and a first doping level, overlying said common region and forming said control regions;

a plurality of conduction regions of said first conductivity type formed in said active area regions and forming said first regions; and

a plurality of control contact regions of said second conductivity type and a second doping level, higher than said first doping level, formed in said active area regions,

wherein each active area region is shared by at least two bipolar transistors.

2. A cell array according to claim 1 wherein said active area regions have a strip-like shape and accommodate each a plurality of conduction regions and a plurality of control contact regions.

3. A cell array according to claim 2 wherein said conduction regions and said control contact regions are alternated, and each conduction region is arranged between two consecutive control contact regions, and each control contact region is arranged between two consecutive conduction regions.

4. A cell array according to claim 2 wherein each control contact region has at least two consecutive conduction regions on each side.

5. A cell array according to claim 2, comprising a plurality of insulating regions having strip-like shape and extending each between two adjacent active area regions.

6. A cell array according to claim 1 wherein said active area regions have a rectangular shape and accommodate each at least two conduction regions and one control contact region.

7. A cell array according to claim 6 wherein said control contact region is arranged between said conduction regions.

8. A cell array according to claim 6, comprising an insulating region having a grid-like shape accommodating and defining said active area regions.

9. A cell array according to claim 8 wherein said active area regions have rectangular shape and are arranged according to a matrix.

10. A cell array according to claim 1, comprising a dielectric region on top of said body; a plurality of first and second electrical contact regions extending through said dielectric region, each said first contact region extending between and contacting a respective conduction region and the first terminal of a respective one of the storage elements, each said second contact region extending from and contacting a respective control contact region.

11. A cell array according to claim 10 wherein said dielectric region accommodates a first and a second plurality of conductive lines, the conductive lines of

said first plurality extending on top of said cells parallel to each other along a second direction, the conductive lines of said second plurality extending on top of said first plurality, parallel to each other along a first direction transverse to said second direction, the conductive lines belonging to one of said first and second plurality of conductive lines being in contact with said second terminals of said storage components and the conductive lines belonging to another one of said first and second plurality of conductive lines being in contact with said second contact regions.

12. A cell array according to claim 1 wherein each said storage component is a phase change memory element of chalcogenic material.

13. A cell array according toclaim 1 wherein said first region is an emitter region, said second region is a collector region and said control region is a base region.

14. A cell array according to claim 1, comprising enriched regions having said second conductivity type and a third doping level higher than said first doping level, said enriched regions extending in said active area regions and being located each below the conduction region of a respective bipolar transistor.

15. A process for manufacturing a cell array, comprising the steps of:

providing a body of semiconductor material of a first conductivity type;

forming a plurality of active area regions of a second conductivity type and a first doping level;

forming, in each active area region, a control contact region of said second conductivity type and a second doping level, higher than said first doping level;

forming, in each active area region, at least two conduction regions of said first conductivity type, each said conduction region forming, together with said active area region and said body, a selection bipolar transistor; and

forming, on top of said body, a plurality of storage components, each storage component having a terminal connected to a respective conduction region and defining, together with said bipolar transistor, a cell of said cell array.

16. The process according to claim 15 wherein said step of forming a plurality of active area regions comprises:

growing insulating regions on said body, said insulating regions surrounding said active area regions; and

implanting said active area regions with doping agents of said second conductivity type.

17. A process according to claim 16 wherein said insulating regions and said active area regions have strip-like shape.

18. A process according to claim 16 wherein said insulating regions form a grid-like structure and said active area regions have a rectangular shape.

19. A process according to claim 16 wherein the conduction regions are formed by implanting dopants of the first conductivity type through a mask, the process further comprising implanting dopants of the second conductivity type through the mask, thereby forming respective enriched regions below the conduction regions and in the active area regions.

20. A memory device, comprising

a plurality of storage components of a plurality of memory cells;

a semiconductor body of a first conductivity type, forming a first conduction region of a plurality of selection bipolar transistors of the memory cells, each of the memory cells including one of the storage components and a corresponding one of the bipolar transistors;

a plurality of active area regions of a second conductivity type, overlying the semiconductor body and forming respective base regions of the bipolar transistors;

a plurality of conduction regions of the first conductivity type formed in the active area regions and forming second conductive regions of the bipolar transistors, respectively; and

a plurality of control contact regions of the second conductivity type and a doping level that is higher than a doping level of the active area regions, formed in the active area regions,

wherein each active area region includes one of the control contact regions and consecutive first and second conduction regions of the plurality of conduction regions positioned on opposite sides of the one of the control contact regions.

21. The memory device of claim 20 wherein the conduction regions and the control contact regions are alternated, and each conduction region is arranged between two consecutive control contact regions, and each control contact region is arranged between two consecutive conduction regions.

22. The memory device of claim 20 wherein each control contact region has opposite sides and the conduction regions include at least two consecutive conduction regions on each of the opposite sides of the control contact region.

23. The memory device of claim 20 wherein the active area regions each have a rectangular shape and each accommodate at least two of the conduction regions and one of the control contact regions.

24. The memory device of claim 20 wherein the memory cells form a memory array that includes rows and columns, each row including a set of the plurality of active area regions, the memory device further comprising an insulating region

separating the rows from each other and separating the active area regions within each row from one another.

25. The memory device of claim 20 wherein each storage component is a phase change memory element.

26. The memory device of claim 20, further comprising enriched regions having the second conductivity type and a doping level higher than the doping level of the active area regions, the enriched regions extending in said active area regions and being located each below the conduction region of a respective one of the bipolar transistors.